

FIG. 1

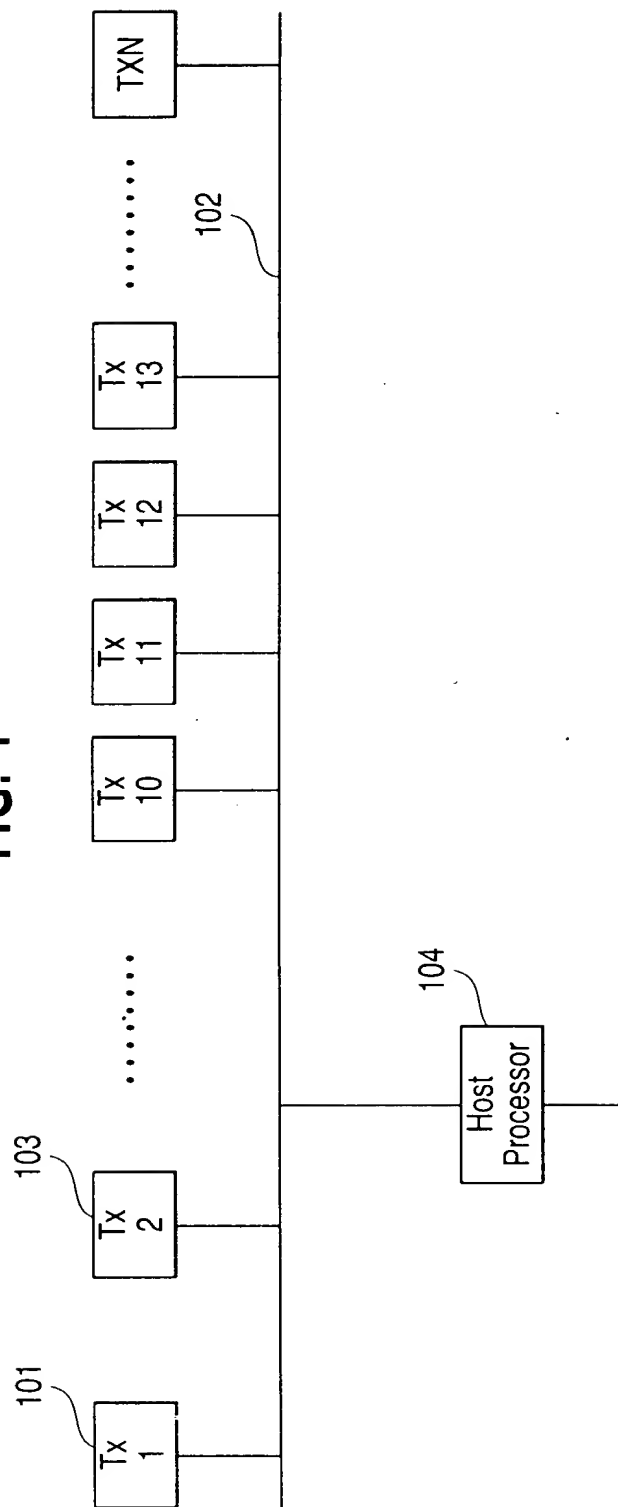


FIG. 2(a)

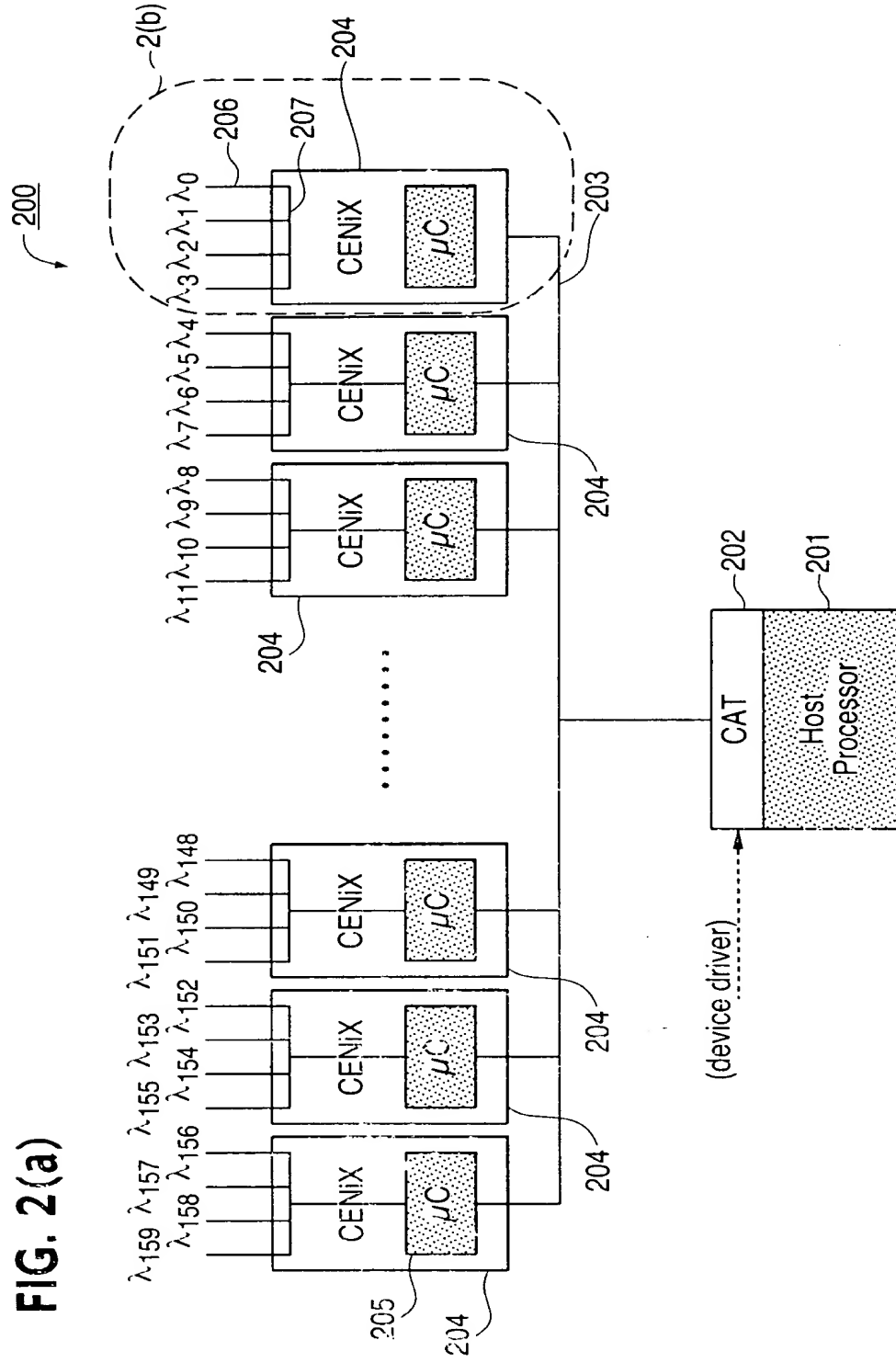


FIG. 2(b)

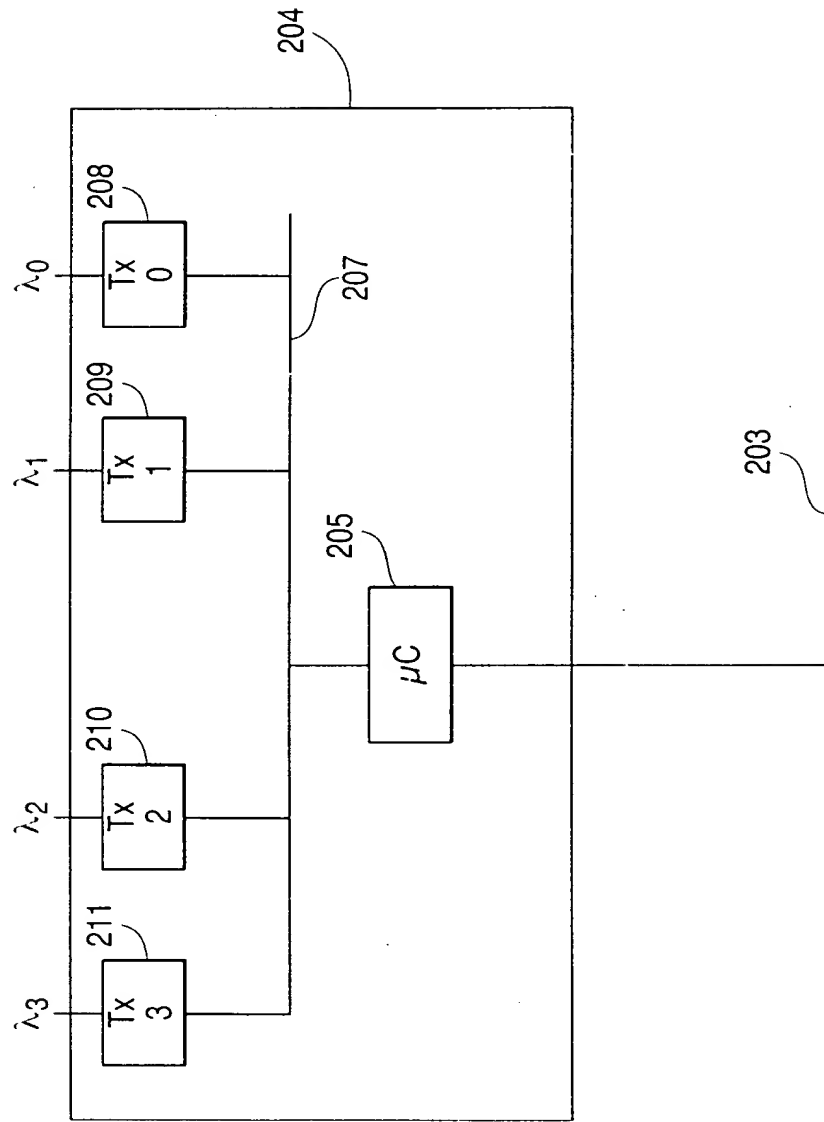


FIG. 2(c)

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(Channel Access Table Example)

Channel Address	Physical Address	Memory Offset
0	0	0x000
1	0	0x200
2	0	0x400
3	0	0x600
4	4	0x000
5	4	0x200
6	4	0x400
7	4	0x600
⋮	⋮	⋮
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

FIG. 3

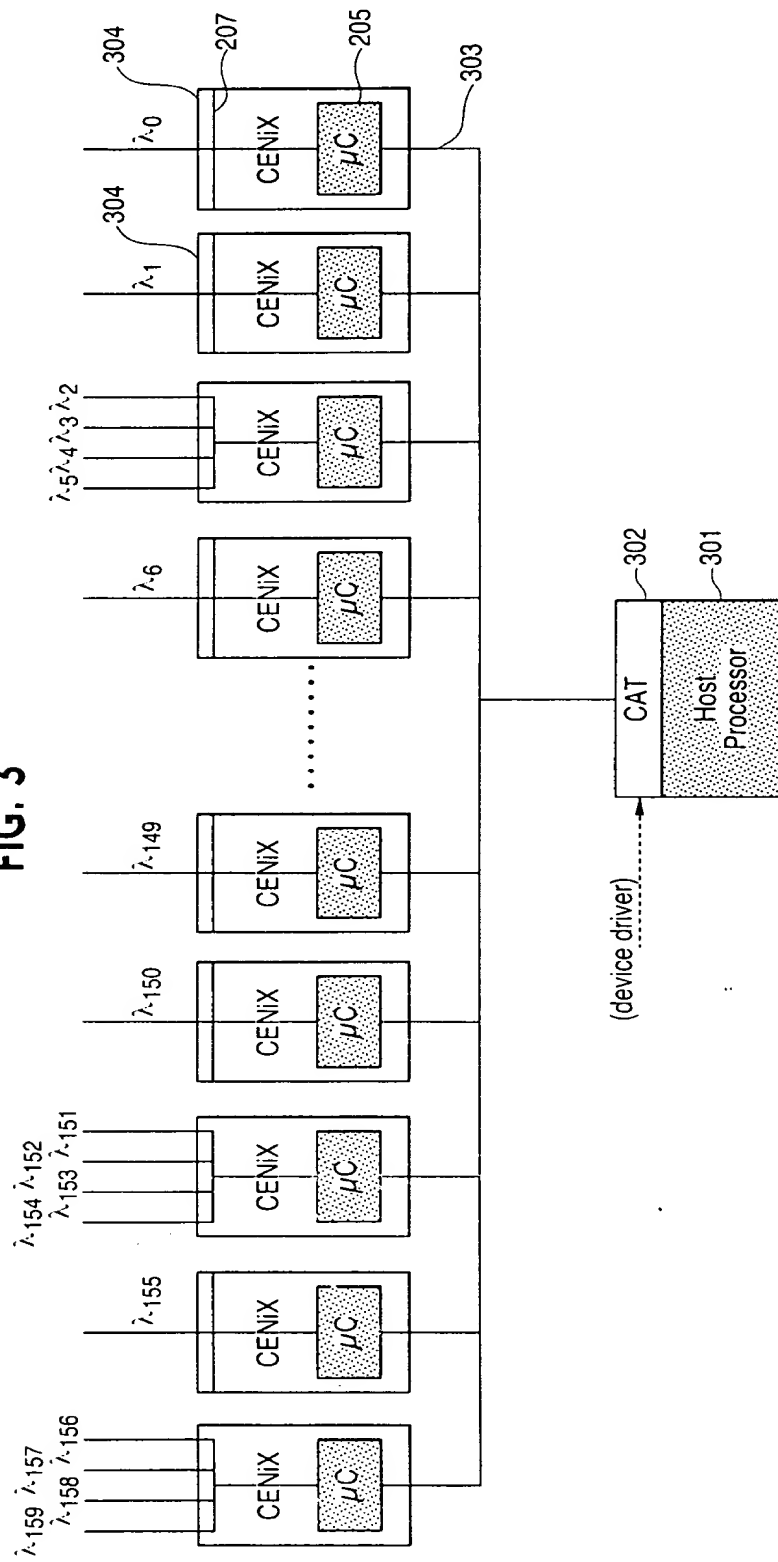


FIG. 4400

(Channel Access Table Example)

Channel Address	Physical Address	Memory Offset
0	0	0x000
1	1	0x000
2	2	0x000
3	2	0x200
4	2	0x400
5	2	0x600
6	6	0x000
⋮	⋮	⋮
154	151	0x600
155	155	0x000
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

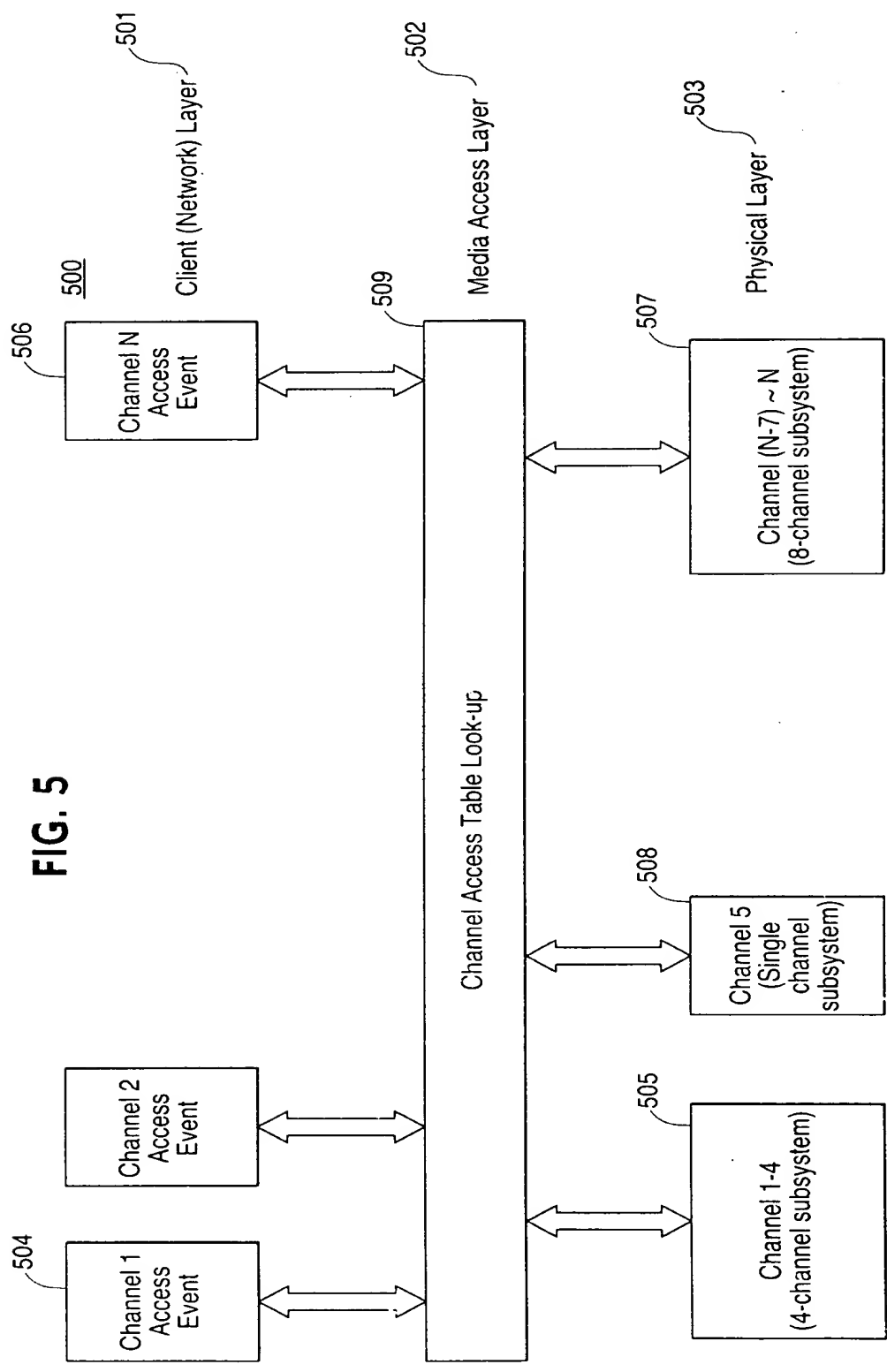
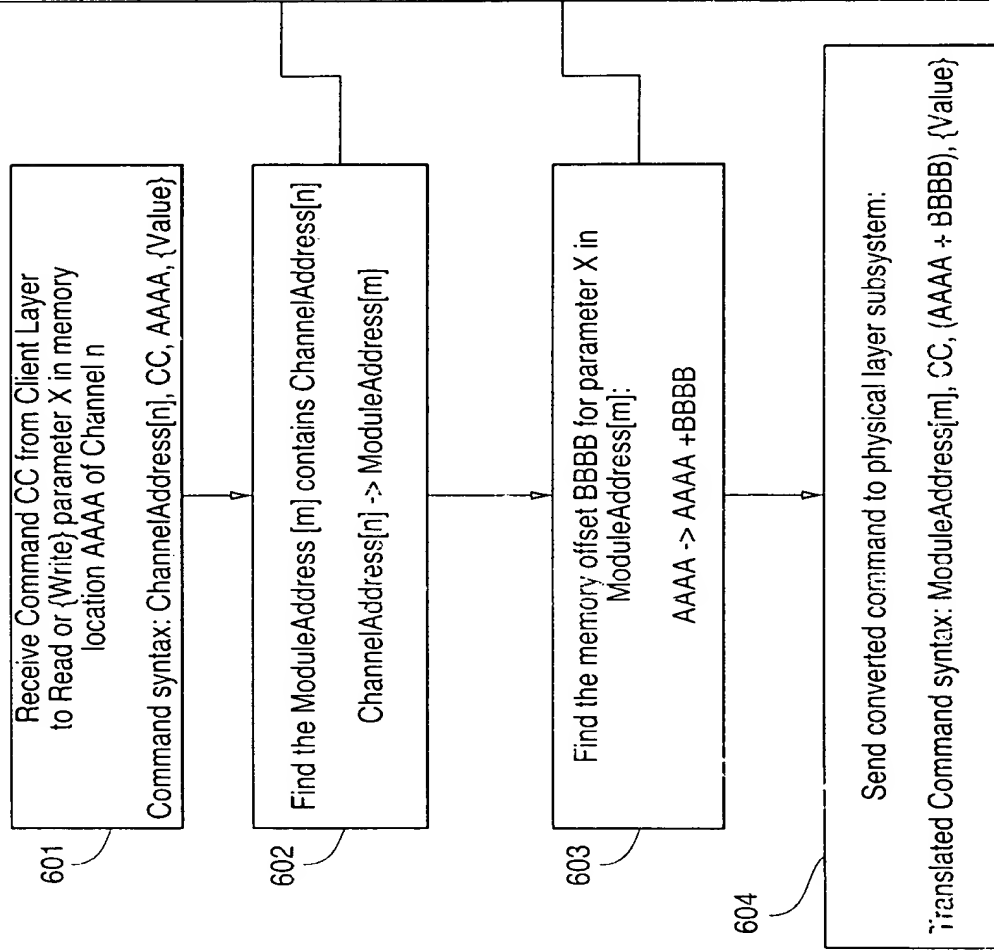


FIG. 6



(Channel Access Table Example)

Channel Address n	Module Address m	Memory Offset BBBB
0	0	0x000
1	1	0x000
2	2	0x000
3	2	0x200
4	2	0x400
5	2	0x600
6	6	0x000
...
154	151	0x600
155	155	0x000
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

FIG. 7

